In the Claims:

1. (Original) A memory cell comprising:

a substrate having an active region defined therein;

a tunnel insulation layer on the active region;

a floating gate disposed on the tunnel insulation layer;

a gate interlayer dielectric layer on the floating gate;

a control gate electrode on the gate interlayer dielectric layer; and

first and second source/drain regions on respective sides of the control gate electrode,

wherein a first one of the active region and the floating gate comprises a portion that protrudes towards a second one of the active region and the floating gate.

2. (Original) The memory cell of Claim 1, wherein the protruding portion tapers toward the second one of the active region and the floating gate.

3. (Original) The memory cell of Claim 1, wherein the tunnel insulation layer is narrowed at the protruding portion.

4. (Original) The memory cell of Claim 1, wherein the active region comprises at least one protruding portion that protrudes toward the floating gate and wherein the floating gate comprises at least one protruding portion that protrudes toward the active region.

5. (Original) The memory cell of Claim 1, wherein the protruding portion adjoins the device isolation layer.

6. (Original) The memory cell of Claim 5, wherein the protruding portion comprises an elongate, tapered region disposed between the device isolation layer and a planar portion of the first one of the active region and the floating gate.

7. (Original) The memory cell of Claim 1, wherein the source/drain regions comprise respective impurity diffusion regions in the substrate.

8-14. (Canceled)